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RESEARCH ARTICLE

DESIGN OF 24 TRANSISTOR STATIC FLIPFLOP AND DIFFERENTIAL CASCODE VOLTAGE SWITCH

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ABSTRACT

In this paper, I have designed a low-power circuit-shared static flip-flop (CS2FF) for low power digital VLSIs. The CS2FF consists of five static NORs and two inverters (INVs).The CS2FF utilizes a positive edge of a buffered clock signal, which is generated from a root clock, to take data into a master latch and a negative edge of the root clock to hold the data in a slave latch. The total number of transistors is only 24, which is the same as the conventional tri-state buffer based flipflop (TBFF) used in the most standard cell libraries. Spectre simulations in 0.18micrometer standard CMOS process demonstrated with different voltages that our proposed CS2FF achieved clock-to-Q delay of 17.4ns, setup time of 5.91ns, hold time of 1.17ns. The DCVS has been designed having less transistors. Cascode voltage switch logic (CVSL) refers to a CMOS-type logie family wich is designed for a certain advantages. It requires mainly N-channal Mosfet transistors to implement the logic using true and complementary input signals, and also needs two P-channel transistors at the top to pull one of the outputs high. This logic family is also known as Differential Cascode Voltage Switch Logic (DCVS or DCVSL).

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INTRODUCTION

Ultra-low power CMOS VLSIs have attracted much attention for use in power-aware applications such as wireless smart sensor networks and implantable bio-medical systems. Several low-power techniques have been investigated. Among them, reducing the supply voltage for digital circuits is the most direct and effective way to achieve low power dissipation because of the quadratic dependence of the power dissipation on the supply voltage. One big issue for ultra-low voltage digital circuits is in the design of a flip-flop (FF) circuit because FFs are widely used in modern digital VLSI systems such a general purpose register, a pipeline register, and a finite state machine. However, their performance tends to degrade at lower supply voltage and moreover, they require a number of transistors to achieve stable and low voltage operation. In light of this background, we herein propose a circuit shared static FF (CS2FF) suitable for extremely low-power digital circuits with a small number of transistors. In light of this back ground, we here in propose a circuit shared static FF (CS^2FF) suitable for extremely low-power digital circuits with a small number of transistors.

The CS^2FF consists of five static NORs and two inverters (INVs). Thus, the CS^2FF uses only 24 transistors. Our proposed FF may achieve clock-to-Q delay of 17.4 ns approx, setup time of 5.91 ns 35approx., hold time of 1.17 ns 35approx., and power dissipation of 15.4 nw, at 0.5-V power supply and 1-MHz clock frequency. The circuit can operate at 0.347 V with an extremely low power dissipation of 6.61Nw.

TIMING DIAGRAM

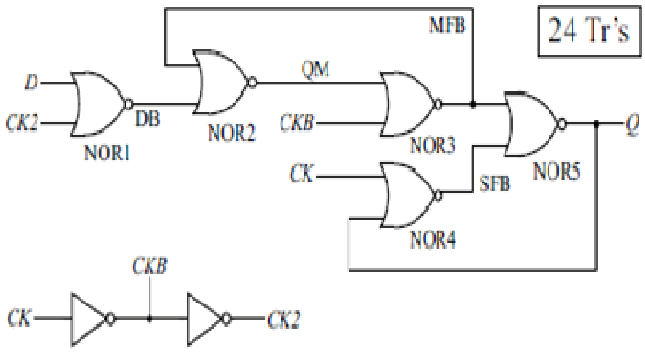

Fig 2.1: CS2FF (Circuit shared static flip-flop)

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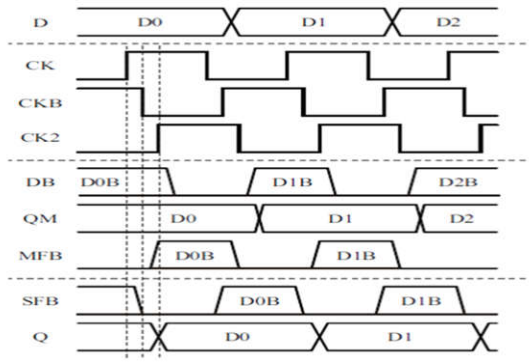

Fig. Timing diagram of our proposed CS^{2}FF

Schematic diagram of CS2FF

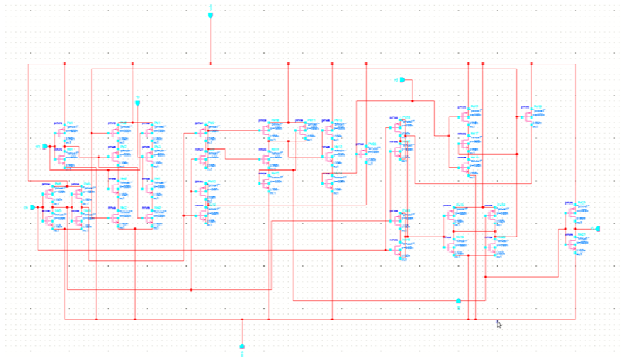

Fig : schematic diagram of CS2FF

Layout design of CS2FF

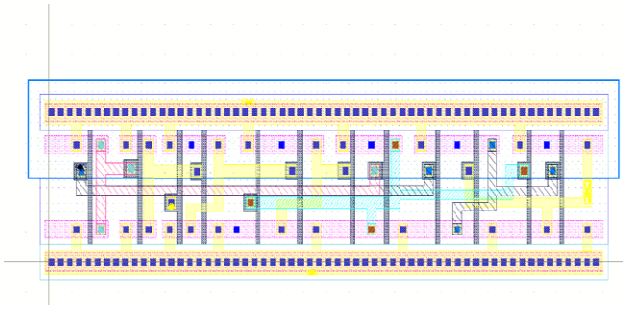

Fig : Layout Design of circuit squared static flipflop

Dcvs (differential cascode voltage switch)

With the advancement in CMOS technology, there is a new interest in designing simple functional units for digital systems. ICs are widely used in consumer electronics, telecommunications and high performance computing. This is to continue with power-efficient VLSI and system designs The Differential Cascode Voltage Switch Logic (DCVSL) is a CMOS circuit technique which has potential advantages over conventional NAND/NOR logic in terms of power dissipation, circuit delay, layout density and logic flexibility. Low-power, circuit design techniques have largely overlooked differential cascode logic circuits (DCVS) in favor of traditional CMOS styles. The high activity of DCVS gates and the need to route differential signals cause them to compare unfavorably with respect to implementations using static CMOS, complementary pass transistor logic, and differential pass transistor logic .However DCVS gates do offer the potential of having high fan-in which leads to a reduction in logic depth, high speed, and the capability of generating completion signals for asynchronous operations.

Simple DCVS structure

In Static logic it consumes no dynamic or static power.it Uses latch to compute output quickly. And requires true/ complement inputs, produces true/complement outputs. Exactly one of true/complement pulldown networks will complete a path to the power supply. Pulldown network will lower output voltage, turning on other p-type, which also turns off p-type for node which is going down.

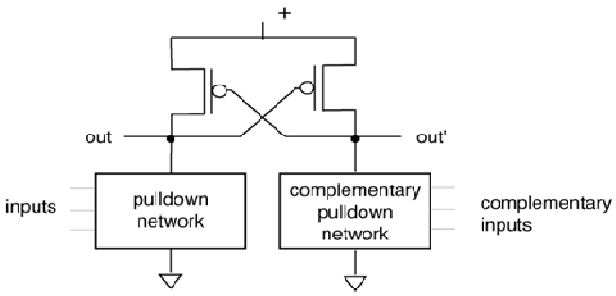

Fig. 3.1.2 Master slave flip-flop

Combine to make a master-slave flipflop

To combine these it works better than single sided flipflops and used fewer. Gates compare to C2MOS. It uses the Smaller clock load. It performs Complementary faster operation

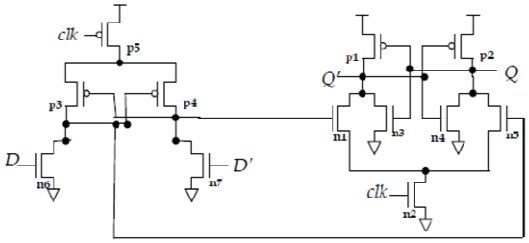

Fig. 3.2. Add Transient response Diagram

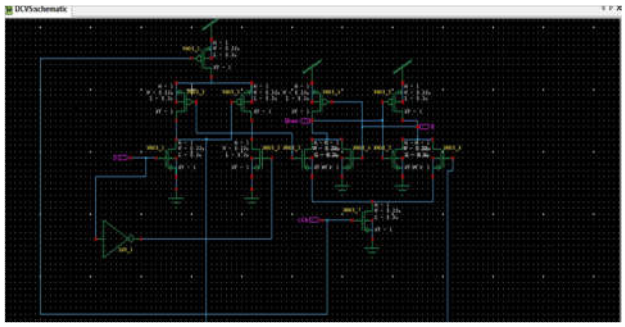

Fig. 3.3. Schematic Diagram of DCVS

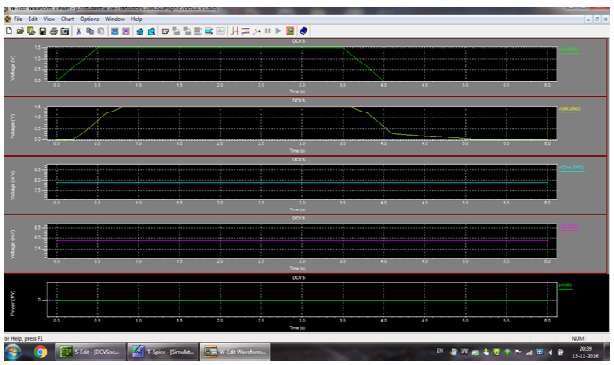

Fig. 3.4. Results of DCVS

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