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REVIEW ARTICLE

DESIGN MULTIPLE VALUE LOGIC FOR FULL ADDER

[1]Mr. A.D. Dhanorkar and *[2]Mr. P. S. Choudhary

[1]M.E Student of PRMCEAM, Badnera-Amravati, (M.S) India
[2]Associate Professor, EXTC Dept, PRMCEAM, Badnera-Amravati, (M.S) India

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ABSTRACT

Many developers have intended their models in binary and quaternary logic using 0.18µm CMOS technology. In Binary logic, circuit has limitations of increase interconnections giving rise to complexities and their by impact on size. Some authors concentrated on put back in place of binary logic with MVL or quaternary logic to prevail over the limitation of size. Second is that for half and full adder (for addition/ arithmetic operations) the quaternary logic method required the conversion of quaternary logic level into binary level for implementation. Our aim is to intend and develop MVL or quaternary logic for full adder without converting these levels to binary logic. It will reduce the one additional step and improve the performance offer less chip size, saving more power. MVL or quaternary logic can be implemented in three different modes. From that mode, voltage mode type model is beneficial to design and give high performance with less dynamic power dissipation. The design is targeted for the 0.18 µm CMOS technology. Design tool for simulation will be ADS (ADVANCED DESIGN SYSTEM) software. We will estimate area, power and delay of the design HAq / FAq without any need of conversion, and compare to existing binary circuits (HAb / FAb).

INTRODUCTION

Multiple value logic are logical calculi in which there are more than two possible truth value. But Logical calculi are bivalent. There are only two possible values for any proposition true and false. Lukasiewiczs was first author who proposed two value and three value logic. i.e (True, false and unknown). Now four value logic i.e quaternary logic concept is new growing technology in VLSI. In this technology more than two value logic is implementing. MVL or quaternary logic means more than two truth value (0,1) logic i.e. n-value logic for n > 2. Here we implement four truth value logic i.e. (0,1,2,3). Several implementation methods have been proposed in the recent papers to realize the MVL circuits (Vasundara Patel and Gurumurthy, 2010; Radanovic and Syrzycki, 1996; Ricardo Cunha, 2007; Hirokatsu Shirahama and Takahiro Hanyu, 2008; Anindya Da *et al.,* 2010). They can fundamentally be categorized as current-mode, voltage-mode and mixed-mode circuits. current-mode circuits (Radanovic and Syrzycki, 1996; Jean-Marc Philippe *et al.,* 2005) have been popular and offer several benefits, the power consumption is high due to their inherent nature of constant current flow during the operation.

Alternatively, voltage-mode circuits consume a large majority of power only during the logic level switching.

Corresponding author: Mr. P. S. Choudhary,
Associate Professor, EXTC Dept, PRMCEAM, Badnera-Amravati, (M.S) India.

Hence, voltage-mode circuits do offer lesser power consumption which has been the key benefit of traditional CMOS binary logic circuits from the perspective of dynamic switching activity. Several approaches for quaternary circuit design have been proposed (Yasuda *et al.,* 1986; Jean-Marc Philippe *et al.,* 2005; Wakui and Tanaka, 1989), in voltage mode technique. Quaternary logic (radix-4-valued) is chosen as the base radix for the work reported here. Using a quaternary radix offers all the benefits of MVL such as reduced area due to signal routing reduction along with the important advantage of being able to easily interface with traditional binary logic circuits. For example a conventional 16 - bit bus (0 and 1) represents 65536 combinations. If we code the output with Quaternary logic (0, 1, 2 and 3), the width of the bus is reduced from 16 to 8. As a result, we can reduce power and area requirement for the interconnection. For the intend the various tools such as HSPICE, COSMOSCOPE, TANNER and ADS tools are available. ADS (Advance design system S/W) tool is popularly used and support the optimization of circuits.

The organization of the paper is as follows: Section 2 explains discussion of previous research related to the proposed work. Implementation of quaternary half adder and full adder is shown in section 3. Conclusion part of the paper is given in section4.

I. Literature review

2.1 Vasundara Patel, k s gurumurthy

"Design of high perfor-mance quatern-ary adders", International Journal of Computer Theory and Engineering, Vol.2, No.6, December, 2010.

THEORY DETAILS

Author presented their work in the quaternary logic or MVL for half and full adder by using Q-B and B-Q conversion technique during implementation. The design implemented in 0.18µm CMOS technology and verified through HSPICE and COSMOSCOPE tool.

OUR FINDING

We find that in this technique during implementation, DLC circuit is used for conversion in intend model. By using conversion technique, intend model could not be achieved high performance (Vasundara Patel and Gurumurthy, 2010).

2.2 Vasundara Patel, k s gurumurthy

"Arithmetic operations in multivalued LOGIC. ", International Journal of VLSI, vol.1, no.1,pp. 21-32, March 2010.

THEORY DETAILS

Author presented MVL for arithmetic operations like addition, subtraction and multiplications by using also Q-B and B-Q conversion in Galois field. They used 0.18µm cmos technology and HSPICE as tool for simulation and Karnaugh diagrams used for minimization of logic.

OUR FINDING

We find that this author implemented MVL or quaternary logic for all arithmetic operations. But they used module-n for conversion technique, so designed model could not be achieved high performance during operation (Vasundara Patel and Gurumurthy, 2010).

2.3 Bob Radanovic, Marek Syrzycki

"CURRENT-MODE CMOS ADDERS USING MULTIPLE-VALUED LOGIC", Canadian Conference on Electrical and Computer Engineering, pp.190-193, 1996.

THEORY DETAILS

Author presented the two design model for adder in current mode MVL. The first design of adder cell uses the radix-2 algorithm and 7 levels of current, fabricated in 0.8µm cmos technology with unit current step is 12µA.

The second design is 4-digit decimal adder with standard algorithm and 10 current levels with 1.5µm cmos technology and 1µA unit current step.

OUR FINDING

We find that two major issues in the design of CMMVL are the numerical representation of numbers and the unit current step per logic level. Because the numerical representation of number uses positive and negative current and unit current step per logic levels uses positive current. Due to inherent nature of current, the intend model is failed to achieve high performance (Radanovic and Syrzycki, 1996).

2.4 Ricardo Cunha, Henri Boudinov and Luigi Carro

"QUATERNARY LOOK-UP TABLES USING VOLTAGE-MODE CMOS LOGIC DESIGN", 37th ISMVL pp.56-56,13-16 May, 2007.

THEORY DETAILS

Author presented a new logic functions, implemented using quaternary lookup tables. In this work, a quaternary multiplexer circuit is designed to implement any n-variable quaternary logic function based on its truth table. All circuits simulated with the Spice tool using TSMC 0.18 µm technology.

OUR FINDING

Quaternary look up table or mux in voltage mode cmos logic, design model gives high performance with less power dissipation and less no. of transistor as compared to current mode CM MVL . But the quaternary multiplexer circuit consists of Down Literal Circuits (Ricardo Cunha, 2007).

2.5 Hirokatsu Shirahama and Takahiro Hanyu

"DESIGN OF HIGH-PERFORMANCE QUATERNARY ADDERS BASED ON OUTPUT-GENERATOR SHARING", 38th ISMVL, pp. 8-13. 2008.

THEORY DETAILS

Author proposed a design model of quaternary full adders based on output generator sharing in CM and VM mode. Arbitrary quaternary functions are performed by converting the quaternary inputs into binary and generating the desired quaternary outputs. The generating of desired quaternary outputs sharing with some processing elements like flip flop, comparators.

OUR FINDING

We find that this proposed model is achieved high performance in voltage mode. The delay and power dissipation of the proposed model in voltage-mode during implementation are reduced to 73 percent and 79 percent, respectively.

But by using I/P conversion technique, interconnection complexity and area/ size increases (Hirokatsu Shirahama and Takahiro Hanyu, 2008).

2.6 Anindya Das1, Ifat Jahangir2 and Masud Hasan

"Design of quaternary serial and parallel adders", 6th ICECE 2010, 18-20 December 2010, Dhaka, Bangladesh.

THEORY DETAILS

In this paper, author provided the necessary equations required to design a full adder in quaternary logic system. They implemented the design of a logarithmic stage parallel adder which can compute the carries within log2(n) time delay for n qudits have limited number of fan-in.

OUR FINDING

We find that, they have utilized the associated algebra to design different kinds of expressions for full adder in quaternary logic system. They have proposed a design of logarithmic stage carry-tree adder which has time delay of log2(n) due to its tree structure (Anindya Da *et al.,* 2010).

2.7 Y. Yasuda, Y. Tokuda, S. Zhaima, K. Pak, T. Nakamura A. Yoshida

"Realization of quatern-ary logic circuits by n-channel mos devices", IEEE Journal of Solid State Circuits, vol.21, no.1, pp.162-168, 1986.

THEORY DETAILS

Author presented a new method, such as inverter, NAND, NOR, and delta literal circuits have been fabricated by conventional NMOS technology in quaternary logic. These circuits are comprised of MOS transistors with three values of enhancement-mode threshold voltage and one depletion-mode threshold voltage.

OUR FINDING

We find that by implementing this method, the main advantage is the small number of MOST's required, using simple layout patterns which allow direct comparison with circuit diagrams, and exact transfer characteristics (Yasuda *et al.,* 1986).

2.8 Jean-Marc Philippe, S´ebastien Pillement, Olivier Sentieys

"A low-power and high-speed quaterna-ry interconn-ection link using efficient converters", ©2005 IEEE.

THEORY DETAILS

They introduce a new quaternary link including a binary to quaternary encoder and a quaternary-to-binary decoder in voltage mode multiple-valued logic (MVL). This link improves the transistor count compared to existing designs and it has no DC current path.

OUR FINDING

We find that, here again use of Q-B and B-Q conversion for designing the encoder and decoder. Whenever the conversion is used h/w complexity, area/size increases (Jean-Marc Philippe *et al.,* 2005.

2.9 Kawahito, S. Kameyama, Higuchi, Yamada IEEE MEMBER

"A 32 X 32-BIT MULTIPLI-ER USING MULTIPLE-VALUED MOS CURRENT- MODE CIRCUITS", IEEE Journal Of Solid-State Circuits, Vol. 23. No. 1, February 1988.

THEORY DETAILS

Author designed A 32x32-bit multiplier LSI with binary input and output has been designed using multiple-valued current-mode circuits and implemented in 2-µm CMOS technology. The multiplier, based on the radix-4 SD number system is realized by a regular array structure using a three-stage binary-tree scheme.

OUR FINDING

We find that, author presented a new design model MVL for multiplier. This model is LSI (large scale integrated) model with large h/w complexity. In this design model CM mode circuit failed to achieved high performance. Due to inherent nature of current (Wakui and Tanaka, 1989).

2.10 Vasundara patel K S. Dr K S Gurumurthy

"MULTI-VALUED LOGIC ADDITION AND MULTIPLICA- TION IN GALOIS FIELD", 2009 International Conference on Advances in Computing, Control, and Telecommunication Technologies.

THEORY DETAILS

Author presented a design model on the basis of MVL for Modulo-4 addition and multiplication. Logic design of each operation is achieved by reducing the terms using Karnaugh diagrams. Hspice simulation tool is used with 0.18µm cmos technology.

OUR FINDING

We find that here again author used a module -4 addition and multiplication. Module-4 operation is used for Q-B and B-Q conversion. Whenever conversion is used design model is failed to achieve high performance (Vasundara Patel and Gurumurthy, 2010).

II. PROPOSED WORK

In this paper we will propose the quaternary half adder and full adder by using quaternary input and will obtained the quaternary output without using any converter. No need to convert the quaternary input into binary or binary to quaternary. From this method we can minimize the h/w implementation, power dissipation of circuit, require less number of transistor and we will achieve the high performance.

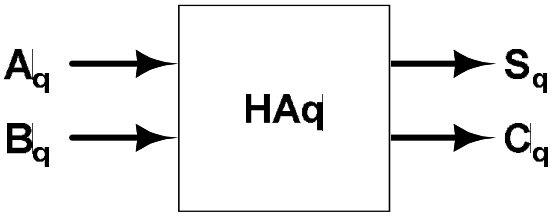

Fig.1. Block diagram of quaternary half adder

Table 1. The truth table of quaternary half adder

A_q	B_q	S_q	C_q
0	0	0	0
0	1	1	0
0	2	2	0
0	3	3	0
1	0	1	0
1	1	2	0
1	2	3	0
1	3	0	1
2	0	2	0
2	1	3	0
2	2	0	1
2	3	1	1
3	0	3	0
3	1	0	1
3	2	1	1
3	3	2	1

I. IMPLEMENTATION OF QUATERNARY / MVL FOR HALF ADDER

In quaternary logic, addition can be performed in many ways. Numbers in quaternary logic can be directly added or numbers in quaternary logic can be converted to binary logic and addition can be performed in binary logic. Binary results of addition can be displayed in quaternary logic after conversion. But we will perform the addition only by using quaternary logic only. In (Vasundara Patel and Gurumurthy, 2009) modulo-4 addition is introduced, implementation of carry without hardware. Figure 1 explains the block diagram of quaternary half adder. In truth table Aq and Bq are quaternary input numbers and Sq and Cq are the quaternary output numbers.

Table 2. Truth tables of quaternary full addition, when carry in is 1

SUM

	Aq				
Bq		0	1	2	3
	0	1	2	3	0
	1	2	3	0	1
	2	3	0	1	2
	3	0	1	2	3

CARRY

	Aq				
Bq		0	1	2	3
	0	0	0	0	1
	1	0	0	1	1
	2	0	1	1	1
	3	1	1	1	1

Table 3. Truth table of quaternary full addition when carry in is 0

SUM

	Aq				
Bq		0	1	2	3
	0	0	1	2	3
	1	1	2	3	0
	2	2	3	0	1
	3	3	0	1	2

CARRY

	Aq				
Bq		0	1	2	3
	0	0	0	0	0
	1	0	0	0	1
	2	0	0	1	1
	3	0	1	1	1

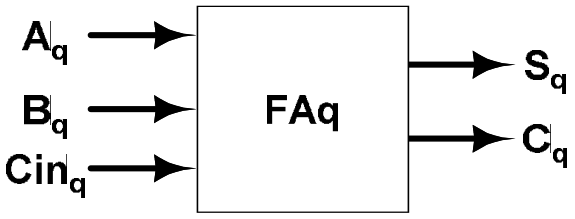

Figure 2. Proposed quaternary full adder

II. IMPLEMENTATION OF QUATERNARY FULL ADDER

Proposed full adder circuit is based on Quaternary adder. Block diagram of the full adder circuit is shown in Figure 2. Aq and Bq are the two quaternary inputs to the full adder. Table 2 shows sum and carry for all possible combinations of inputs when carry input is one. Table 3 shows sum and carry for all possible combinations of inputs when carry input is zero. Aq, Bq and Cin q are quaternary input numbers and Sq and Cq are the quaternary output numbers.

Conclusion

In this paper we review the historical developments in this field, both in circuit realizations and in methods of handling multiple-valued design circuit. In the recent years MVL gaining the importance due to its inherent benefits like high speed, low area, and low dynamic power dissipation (VM), we found during analysis of MVL, it has great high message communication ability. In earlier work quaternary logic or (MVL) (Vasundara Patel and Gurumurthy, 2010; Radanovic and Syrzycki, 1996; Ricardo Cunha, 2007; Hirokatsu Shirahama and Takahiro Hanyu, 2008; Anindya Da *et al.,* 2010; Yasuda *et al.,* 1986; Jean-Marc Philippe *et al.,* Wakui and Tanaka, 1989; Vasundara Patel and Gurumurthy, 2009), arithmetic operations like addition, subtraction and multiplications presented which use Q-B conversion, B-Q conversion for implement the arithmetic operation. We proposed half adder and full adder in quaternary to quaternary

without any conversion which then lead more optimization at farther level.

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