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RESEARCH ARTICLE

VHDL MINIATURIZATION OF AN ELECTRIC REHABILITATOR WITH DYNAMIC CONTROL

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ABSTRACT

Electronic systems are becoming more compact thanks to technological development. Integrated technology provides electronic systems that are more and more thumbnails, economical and robust for different operating conditions. Biomedical technology and especially the electrical stimulator are also concerned by the embedded technology to provide a portable, inexpensive and most flexible and efficient in terms of accuracy and speed. In this work, we present a new VHDL modeling of an electrical rehabilitator from an original design. First, we propose an integrated architecture to reduce the electrical stimulator. We will discuss the operational units and their main functions. Then we present a reduced interface well suited to the portability of the device. The reduced system contains tow global blocks of analog and numerical treatment. This last one constitutes the main of this study and it consists of six blocks to generate stimulus signal and the command signal. The interface adopts two types of manual and automatic amplitude control in order to control the stimulation signal, and allows the setting of the stimulation training.

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INTRODUCTION

Miniaturization is a technical design in electronics at the Micro (10^{-6}) or Nano (10^{-9}) scale. It is programmed and synthesized with so-called specific languages or language description Equipment Hardware Description Language (HDL). VHDL (VHSIC Hardware Description Language) is an HDL language designed to represent the behavior and the architecture of a digital electronic system. A specification described in VHDL can be checked by simulation before the detailed design is completed. In addition, the computer-aided design tools that make it easy to move directly from a functional description in VHDL to a gate pattern have revolutionized methods of designing digital circuits, ASIC or FPGA. And a miniaturization with these technologies allows reducing:

- Occupied space and weight;
- Construction cost;
- Energy consumption ;
- Material consumption.

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The reduced energy consumption of FPGA technology promotes independence and portability of the device. And prototyping on FPGA provides more flexibility in electronics development. With these advantages, and with a dynamic architecture, the electrical stimulator may be compact, portable and multi-functional. The miniaturization of electrical stimulation systems provides flexibility to integrate electronic systems in everyday life by transcutaneous settlements (Guiraud *et al*., 2006; Andreu *et al*., 2005; Liu *et al*., 2008; Boyer and Sawan, 1995), and with the integrated description of the FPGA, it allows better control settings of electrical stimulation and have an autonomous and intelligent device (Ngamkham *et al*., 2016; http://www.freedomfchs.com/pcofthemindbydrjosed.pdf; Ham *et al*., 2006). In this work, we present HDL architecture of an electro-stimulator. The system designed here permit to have an accurate and a dynamic setting option to expand the therapeutic applications of our rehabilitator.

Description of the architecture

The electrical stimulator proposed in (Salbi and Bri, 2014; Salbi and Bri, 2016) is based on the generation of two rectangular signals V1 and V2. These pulses are amplified in power and then controlled in amplitude by the control stage.

The generation of the clock signal and the logical sequencer are established by the integrated circuit NE555. The automatic control is generated by a digital module and converted via a digital to analog converter (DAC). In order to reduce the electrical stimulator, we propose the architecture shown in Figure 1, in which we collected the generator of the stimuli (V1 and V2) with the digital control unit in a single module called digital part.

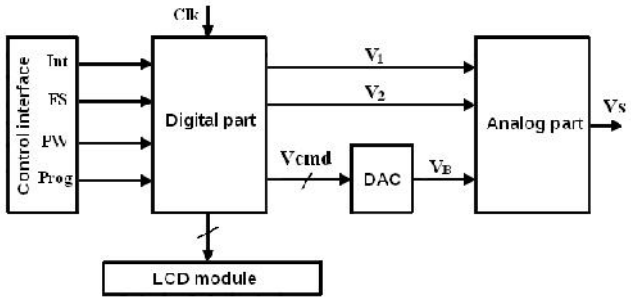


Figure 1. Block diagram of miniaturized stimulator

The analog part remains the same as was described in (Salbi and Bri, 2014). It consists of a power stage and a boosting transformer with a midpoint. The DAC performs the digital to analog conversion and also a voltage-current with a resolution of 8 bit. The digital part is synthesized by VHDL. Figure 2 shows the functional structure. It consists of a pulse generator with a frequency divider (Stim_freq), a pulse width controller (Stim_width), a logical sequencer (Sequencer), a control unit (CPU) and a memory for storage (ROM).

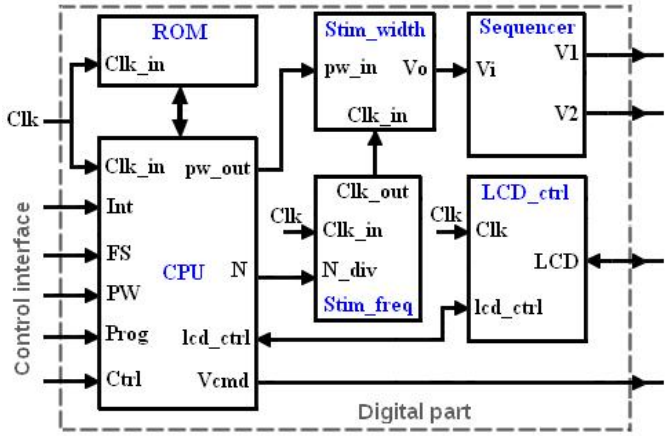


Figure 2. Proposed architecture for the digital part

We consider an user interface that would be described later in this paper. We first start with the sub-blocks of the digital part.

Frequency divider

The Stim_freq block allows imposing the frequency of stimuli from the user selection on the FS entry. This is a programmable frequency divider (Figure 3). Its entrance is a fixed clock signal. The FS value determines the ratio of the frequency divider (N or N_div). The output signal is a clock signal (Clk_out) of frequency given by Equation 1:

$$Clk_{out} = \frac{Clk_{in}}{N} \quad (1)$$

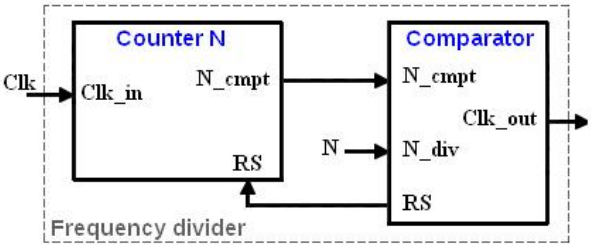


Figure 3. Block diagram of the frequency divider

Generaly the value of N can be any positive integer. This coefficient is calculated in the CPU block from the desired frequency FS, using Equation 2:

$$N = \frac{Clk}{FS} \quad (2)$$

Where, the parameter Clk is the clock frequency, andit is fixed in advance.

Thus, the counter is counting up to N_cmpt. The comparator compares the counter output value with that of N. Once N_cmpt = N / 2, it triggers the high state of new clock signal Clk_out and the counter resets to zero by RS signal. Studies that are made on that stage (Kovacheva *et al*., 2014; Moon *et al*., 2005; Meng *et al*., 2009) showed that most of the frequency dividers are implemented with an even coefficient N. As well as the divider with an even coefficient is easy to realize it is imprecise in terms of resolution as square waves, that is to say to have a δ duty factor of 50%. This is an essential parameter for the frequency dividers. It is highly desirable that the output signal preserves the duty cycle of the input, especially when δ = 50%. This is very important for applications such as clock generation and frequency synthesizers when specific types of phase detectors are used (Kovacheva *et al*., 2014); or when the time shift is critical as the case of the pacemaker. The process of designing a frequency divider with even coefficient N and with a cyclic coefficient of 50% is a trivial task. It is performed usually with a programmable counter working only on the first edge of the input clock signal. In this case, the frequency of the output signal is given by equation 3:

$$Clk_{out} = \frac{Clk_{in}}{2N} \quad (3)$$

The problem which may prove here is when the coefficient N is odd. In other studies we have discussed this with odd N (Kovacheva *et al*., 2014; Moon *et al*., 2005; Meng *et al*., 2009; Tseng *et al*., 2009; Magoon and Molnar, 2002), and has proposed various solutions. The more efficient that appears to us is that described by Kovacheva *et al*. (2014). In their study they propose a general architecture for whatever positive integer N the frequency divider will have a cyclic factor of 50%. The limitation of this proposal is the frequency margin in which the division error is acceptable. The frequency margin is capped by 10 MHz. Fortunately we work with a very low frequencies that not exceeding 500 Hz if necessary. Thus we ignored this limit. If N is even the switch (SW) switches to N_{even} and output uses the simple counter in left that counts up

to N/2. When N is odd, the switch SW switches to N_{odd} and run the algorithm (right) who has two counters, one account on the falling edges and the other account on the ascending fronts to N. We have improved this architecture; and we have adapted its blocks with the overall system. This brings us to the architecture of Figure 4.

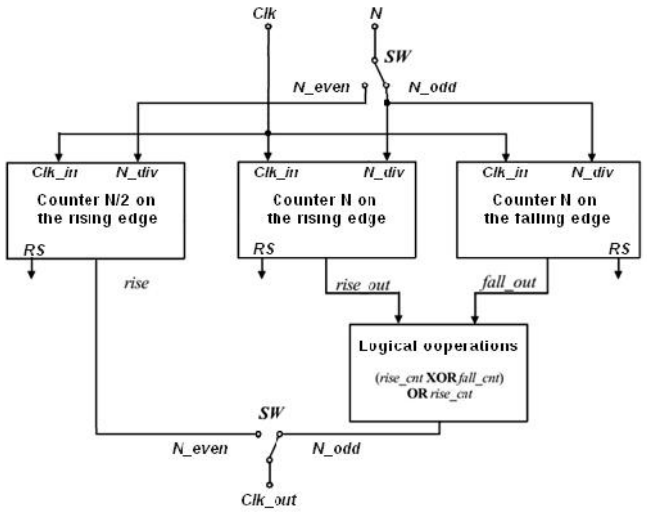


Figure 4. Proposed Architecture for the frequency divider

We have added a switch (SW) early in the process. By checking the parity of the factor N in the beginning we can avoid unnecessary calculates counters. Also, we do not need a block reset because it is integrated into the architecture of the CPU.

Stimulus width controller

The Stim_width block is to generate a pulse of width determined by the user. It is a programmable delay generator; its operating frequency is set by the FS block. The output is an electrical stimulus of a PW(us) and a frequency FS(Hz). The most critical parameter in this block is the time; we should generate an accurate and editable delay. Obviously FPGA technology provides high temporal precision as it provides parallel compute. They exist several architectures to generate the delay offering better accuracy in high frequencies (Hormot *et al*., 2015; Koutroulis *et al*., 2006; Zhaolin *et al*., 2010). These studies are based on frequencies of the order of tens of mega-Hertz, but they are working with the same principle; the process is based on a counter and a comparator or with the principal of pulse-width modulation (PWM) (Larson, 2015). The counter counts until the comparator detects the time that defines the pulse width (PW), and at that time it sets the output to the low state. Figure 5 explains chorographic scenario.

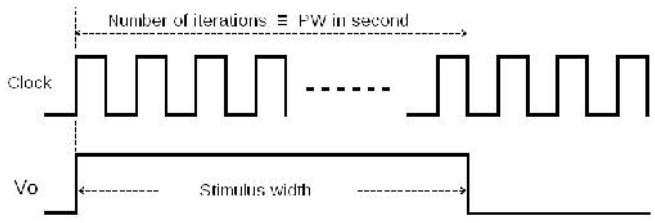


Figure 5. Chronograph block of Stim Width

The Clk_in triggers the impulse and the internal counter starts timing at the frequency of clock signal Clk to obtain the maximum accuracy. In the architecture of our rehabilitator, the operating frequency is very low (1-500 Hz) in comparison with the frequency of the system clock (20 MHz or more).

Logical sequencer

On the next stage, the Sequencer block reconstructs the same stimulus (Figure 6) with time shift duration PW (us) is the same duration as the stimulus width. On the output, there are two identical signals V_1 and V_2. These two signals will concatenate on power stage (analog part) to get one bipolar and symmetrical signal.

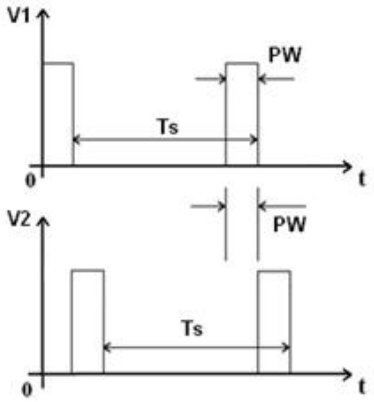


Figure 6. Signals of the logical sequencer

The signal V_1 is the exciting phase of the signal V_S. The V_2 signal cancels the electric charges after stimulation phase, it is called discharge signal. On this floor we work with the frequency FS fixed by the block Stim_freq, and the functioning of this stage depends on the floor above (Stim_width). In addition the principle of logical sequencer is based on the principle of pulse width controller (Stim_width).

Control unit

The CPU block is the orchestra of all the digital part. It allows the management of the user interface and communicates the input parameters for each system device. Moreover, it takes care of generating the digital signal amplitude control, which will be converted by the DAC. This block considers several input parameters. The clock signal (Clk), the stimulus frequency (FS), the duration of stimulation (PW), the stimulus program and various control buttons. From these parameters, the CPU charged of display on the LCD. After validating the characteristics of the stimulation signal, each parameter is communicated to the concerned block to begin the process. The architecture we propose is sequential in the chain: frequency divider, width controller, and logical sequencer. However, V_{cmd} control signal generated by the CPU must be synchronized with the signals V_1 and V_2. The purpose of the synchronization here is to avoid the amplitude difference between the stimulation phase and the discharge phase because a small difference can cause over time accumulating of electrical charges and polarizing electrodes of the electro-stimulator (Donfack, 2000).

Memory storage

The memory storage can be internal (embedded in FPGA) or external (such as EEPROM). In the case of the EEPROM, the protocol needs to be defined by two lines of I2C communication. Because, it is the best way to communicate between two integrated circuits; and the majority of the embedded memories use this protocol. To simplify the implementation of the system we use here the internal memory (ROM). The ROM is equivalent to a single Look Up Table (LUT) for each combination of input values, an output value is associated (Airiau *et al*., 1998; Wilson, 2016; Subhadra, 2013). The combination of inputs constitutes the memory box address to which we wish to access. We describe materially internal memory with an array of two dimensions and an 8-bit word. We chose a size of 10x7 words, that is to say 10 lines and each line contains 7 words (integer). These seven words are, respectively, the stimulation frequency, the width of the stimulus and the temporal parameters of a stimulus program, which are: T_C, T_M, T_D, T_R and the T_P (time of program training). The communication between the control unit and the memory is described by the block diagram in Figure 7.

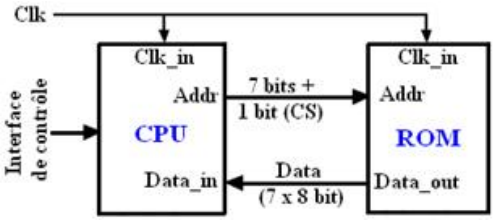


Figure 7. Reading of memory stimulation program

The command to read memory is generated by the CPU via the Addr port. The ROM block receives the address of the line to read with the read command CS = 1. The following flowchart in figure 8 clarified this process.

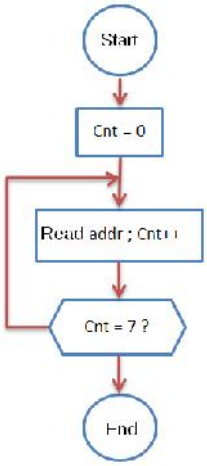


Figure 8. Reading flowchart of the program memory

The received address is the index of the line of 7x10 pictures. Thus, the process reads a line (array) of 7 integer elements. Then, the process sends value by value and each time increments the counter (Cnt) until achieve the seventh element of the line.

User interface

To configure this electric rehabilitator, we considered a simple interface based on a keyboard and a LCD display. We have two choices, either using a program already stored in memory or enter settings program voluntarily by keyboard. For this we propose the design shown in Figure 9.

Figure 9. Interface of the Electrical rehabilitator

In this design, we insisted to the ergonomics of the interface to facilitate user interaction with the electrical stimulator (Jung and Kee, 1996; Oborski, 2004; Yan, 2011). For the output device we used the LCD module 16x2 types. This module is widely used in electronics having regard to its easy integration and its low cost. The input device is a keyboard of nine buttons and a logical switch. The Int. LCD switch turns on/off to consider the reduced interface or the GUI on computer. The buttons below LCD are used to select various settings displayed on the menu. There are directional buttons to navigate through the submenus or configure a setting. The OK button is to enter the selection, configuration, or start / stop running, while the Ret button is to go back in the menu or cancel a setting. According the specifications of the LCD (16x2), it has a communications protocol and special management (Hitachi, 2016). Figure 10 shows the various communications between the control unit and this module.

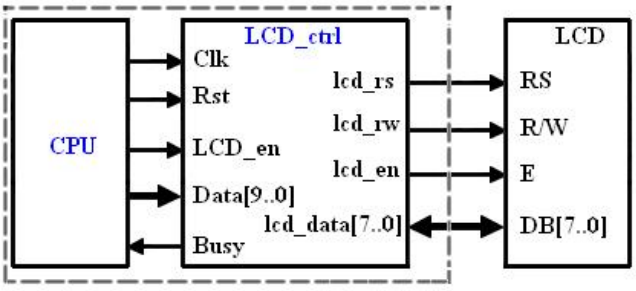


Figure 10. Controller LCD module

The pins used on the LCD screen are standardized to accommodate its use with all electronic circuits (Hitachi, 2016). The display is controlled by sending signals from the microcontroller (CPU) that implements a state machine (figure

11) to send data to display on the screen and / or reading what is displayed there (Larson, 2016).

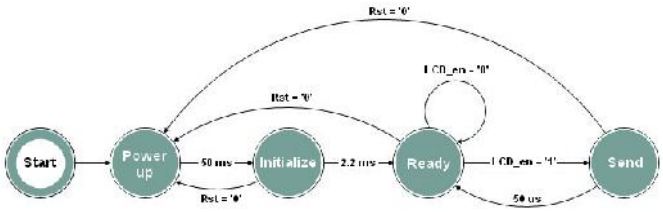


Figure 11. State machine for managing the LCD

The status of the display controller machine (LCD_ctrl) consists of five states. First, we activate the reduced interface with the switch Int._LCD, this starts immediately the system, it awaits a 50 ms to ensure the stability of the supply voltage. Then we proceed with the initialization of the LCD by all necessary configurations described in the specifications of the LCD datasheet. This process can be performed in about 2.2 ms. Then the controller assumes the disposal of the module. In this state, we have only to assert the lcd_en port to activate the final state which ensures the sending data. Figure 12 shows the timing diagram of the data sending sequence to the LCD module. The enable port is enabled for a period of approximately 60 microseconds. During this time we can start sending data to write. RS and R / W respectively entries must be in the high and low during the reception (1200 us) (Lattice Semiconductor, 2013).

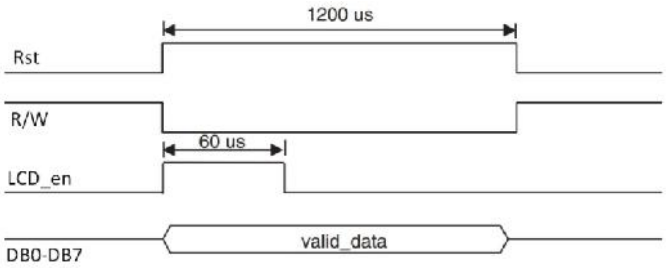


Figure 12. Write timing diagram for the LCD

The combination (Rst = 1; R / W = 0) means that we are in the writing phase in the LCD module. The times recorded on the chart are required by the manufacturer in the datasheet to ensure the good functioning of the component. The general operation of the control unit is designed to make it easier for the user to program the rehabilitator device to the desired application. The user is prompted via the reduced interface to choose a preset program on the memory, or to program his own training rhythm. Then the CPU is responsible for generating a digital signal (V_{cmd}), which describes the amplitude control signal. The following flowchart (Figure 13) simplifies the programming process of the automatic stimulation.

First, in this algorithm we planned to leave the choice to the user, between the LCD interface if portability is required or extended via LabVIEW interface and a computer, it is the role of the transition ' Int.LCD? '. Then, the algorithm offers a choice via the LCD or selecting a predefined program, and there associated parameters is access to the program memory and read; or neglecting the memory and then we go to settings program by using the control buttons. In both choices, the user must validate the stimulus program before running it or return to the menu. We note that the digital part described by VHDL is to be implemented on FPGA and it only works with low voltage, of the order of 3.3 to 5 V. However, the analog part requires a voltage that rises up to 9 or 12 volts in order to have high voltage stimulation. For that it had to think about a power stage which ensures the two sources of tension. Thus, we suggest adding voltage regulator 9 V - 5V. Therefore, the system can be normalized to a supply of 9 V.

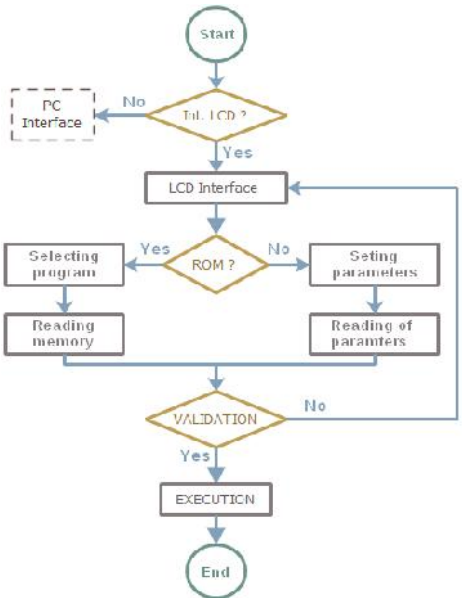


Figure 13. Process operation of the user interface

Synthesis and results

We have described the VHDL hardware on Xilinx ISE software. According to the manufacturer of that software, the synthesis stage receives as input the VHDL code after checking and simulating the constraint file. Figure 14 illustrates the RTL diagram of the digital part of the stimulator. The inputs are represented on the left and outputs on the right.

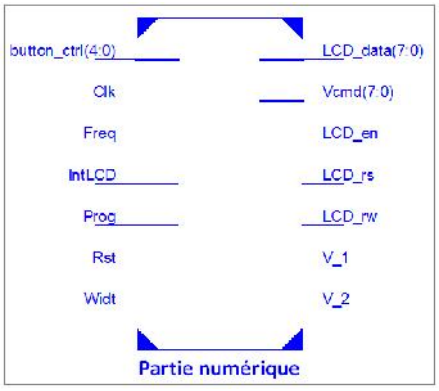


Figure 14. Block of the digital part

Figure 15 presents the internal architecture of this block and the various interconnections of sub-blocks.

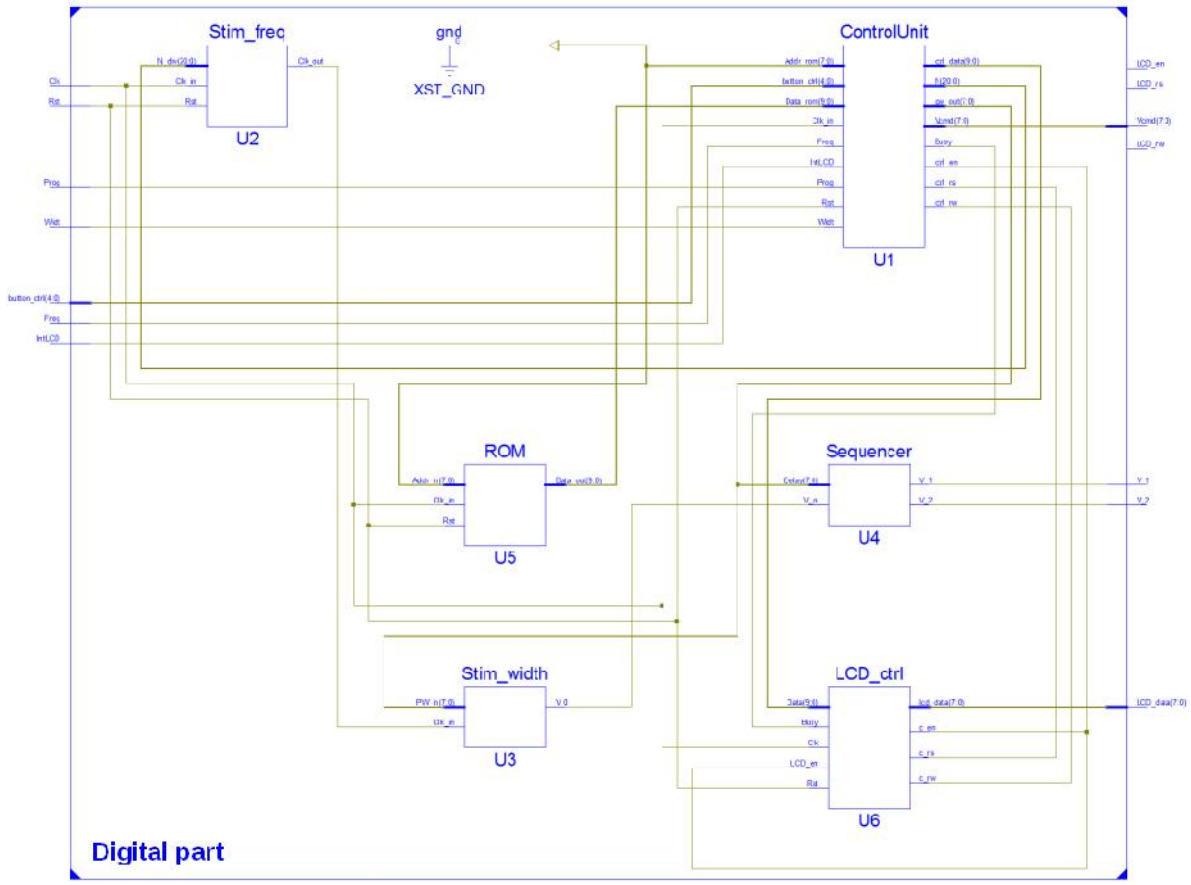
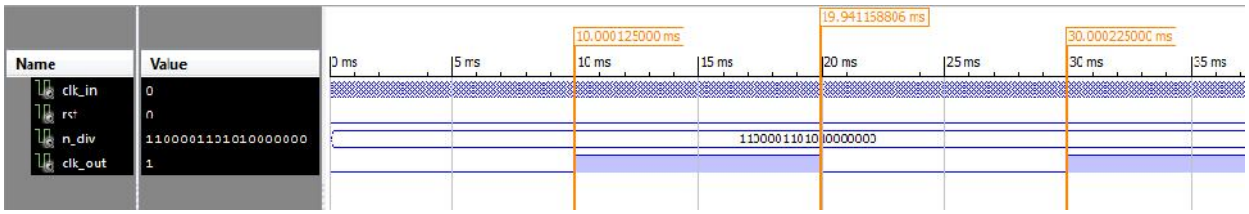
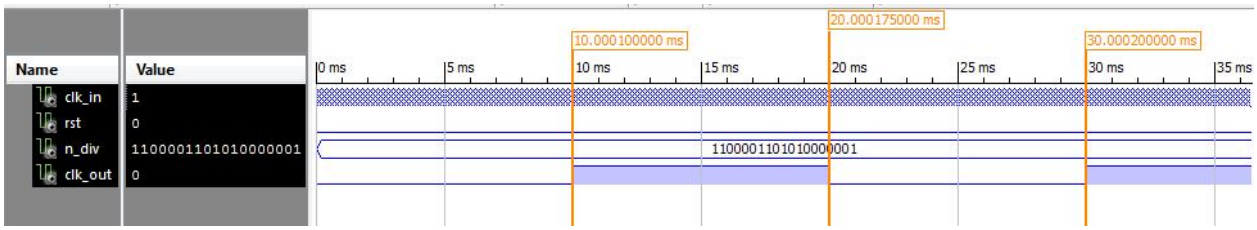


Figure 15. Internal view of the digital part



(A) Simulation for N = 400000



(B) Simulation for N = 400001

Figure 16. Simulation of the frequency divider for even and odd entrance (N)

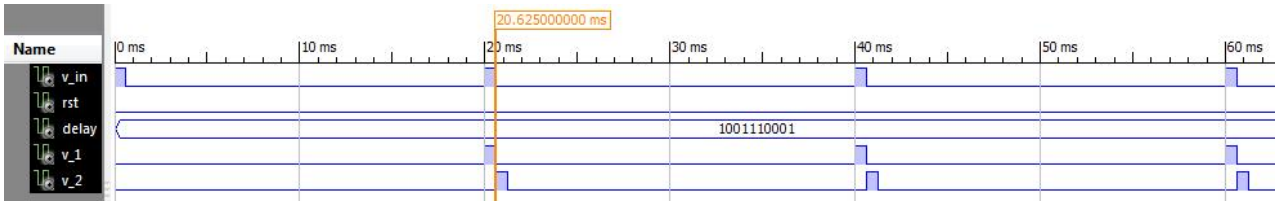


Figure 17. Simulation of the blocks Stim_width and Sequencer

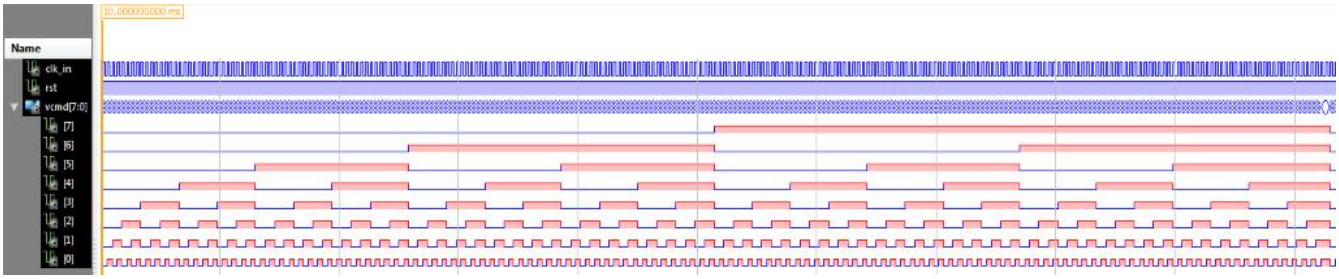


Figure 18. Simulation of digital control in contraction phase

The internal view of the stimulator consists of six blocks. We mainly interested in the simulation blocks: frequency divider (U2), the controller of the duration of the stimulus (U3), the sequencer (U4) and the amplitude controller that is integrated in the control unit (U1). Figure 16 shows the simulation of the block U2 for two divisions (n_div); one is even (A) and the other is odd (B). The frequency is defined by the input clock (clk_in) which is 20 MHz. The comparison shows that the frequency of the output signal (clk_out) is 50 Hz with a duty cycle of 50% and with an error of 0.5%. Figure 17 below shows the result of simulation of the blocks U3 and U4. This timing makes clear that the stimulus width is 625 microseconds just as we set it at the entrance. Moreover it is clear the shift between the signals V_1 and V_2, which is the same value as the pulse duration (625 us). The frequency in the two blocks is the same set to 50 Hz by block U2. The change in stimulus width as well as the sequencing of V1 and V2 is independent of the frequency FS. However the stimulus frequency set by the U2 stage is, somehow, the clock of the U3 and U4 blocks. The digital signal to control the intensity is generated by a process in the block of the control unit. The resolution of the control signal is 8 bits to be compatible with the analog digital converter used in this project. Figure 18 illustrates the chronological evolution of the V_{cmd} Port (8 bits) during the contraction phase. The chronological evolution of V_{cmd} Port is done through a concatenation of the up / down counting process. In this illustration of the contraction phase, we have a digital count from 0 to 255. This is followed by a stabilization of the counter to the maximum value (255) during the maintenance phase. Then the down counting process is running during the relaxation phase to reach the minimum value (zero). Finally, the minimum value is kept during the rest phase. These values are converted via the DAC to voltages ranging from 0 to 9 volts, which involves a resolution of 0.035 V. Of course, this is only the voltage of the control that is to say the stimulus before the amplification stage. However, after amplification by the booster transformer, we will have a voltage between 0 and 90V for a transformation coefficient equal to 10. In this case the resolution is of the order of 0.35 V. This value represents the transition step between stimulation levels and the degree of precision of the level of muscular contraction caused, that is to say strength levels generated by the stimulated muscle.

Conclusion

The miniaturization of the rehabilitator has opened other doors for applications in the medical field. As we have previously mentioned the description using VHDL made the device more flexible thanks to the dynamic programming of the control amplitude and the frequency margin and pulse duration that are sufficiently flexible and broad to cover many therapeutic applications.

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