



RESEARCH ARTICLE

DESIGN AND IMPLEMENTATION OF ALU BY USING GDI TECHNIQUE IN 45 NM TECHNOLOGY

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ABSTRACT

With increasing contribution of performance of digital circuits is judged by its speed, run-time leakage control techniques are becoming extremely important. The most common technology for designing digital circuits is the CMOS technology. After the development of CMOS logic, there was increasing need to optimize circuits in terms of speed. One technique thought was using PTL which makes use of lesser number of gates to realize an operation. The Pass-Transistor Logic (PTL) is a better way to implement circuits designed for low power applications. Although PTL has disadvantages like it reduces the circuit speed at low power operations and greater static power dissipation. As the technology is growing gained the prominent importance. In this design of 1 bit ALU, GDI technology has been deliberately implemented. In this research work a new design of ALU by using GDI technique that can be used to design fast and low power circuits using lesser number of transistors. The total Design of ALU has been done by using GDI technique in 45 nm technology. The total Design process flow in Soc and the power is 0.044.

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INTRODUCTION

An Arithmetic and Logic Unit (ALU) is a digital circuit that performs arithmetic and logic operations. The ALU is a fundamental building block of the central processing unit of a computer. The power consumed by the ALU has a direct impact in the power dissipated from the processor. Hence, a design is required to implement the ALU in a fashion where the performance of the processor is improved and also the power consumed is less. To be precise Power consumption of whole data path can be reduced by reducing power consumption of ALU.

GATE DIFFUSION INPUT (GDI)

The GDI cell is similar to a CMOS inverter structure. In a CMOS inverter the source of the PMOS is connected to VDD and the source of NMOS is grounded. But in a GDI cell this might not necessarily occur. There are some important differences between the two. The three inputs in GDI are namely- 1) G- common inputs to the gate of NMOS and PMOS 2) N- input to the source/drain of NMOS 3) P- input to the source/drain of PMOS Bulks of both NMOS and PMOS

are connected to N or P (respectively), that is it can be arbitrarily biased unlike in CMOS inverter. Moreover, the most important difference between CMOS and GDI is that in GDI N, P and G terminals could be given a supply VDD or can be grounded or can be supplied with input signal depending upon the circuit to be designed and hence effectively minimizing the number of transistors used in case of most logic circuits (eg. AND, OR, XOR, MUX, etc). As the allotment of supply and ground to PMOS and NMOS is not fixed in case of GDI, therefore, problem of low voltage swing arises in case of GDI which is a drawback and hence finds difficulty in case of implementation of analog circuits.

FUNCTIONALITY OF GDI

The most common problem with PTL technique is its low voltage swing. An extra buffer circuitry may be used additionally to eliminate the problem of low swing and improve drivability. The problem of low swing can be understood with the help of a random function. The problem of low swing occurs only when A=0 and B=0 where the voltage level is VTP instead of 0. This occurs due to the poor high to low transition characteristics of PMOS. In the rest of the cases it provides full swing.

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Table 1: Functionality Of any Random Function using GDI

A	B	Functionality	Logic
0	0	pMOS Trans Gate	V_{TP}
0	1	CMOS Inverter	1
1	0	nMOS Trans Gate	0
1	1	CMOS Inverter	0

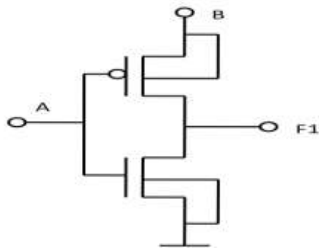


Fig 1. Schematic of any random function

IMPLEMENTING GDI

The below diagram shows the comparative study between GDI and CMOS for AND logic gate showing their schematics. Table1 shows the transient responses of different logic gates using GDI. Table 2 represents the delay and power-delay product results of logic circuits using GDI and CMOS showing GDI as the one with lesser delay or power-delay product

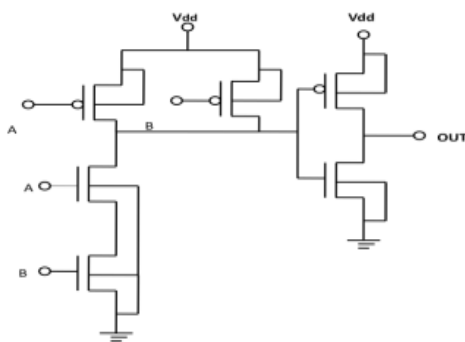


Fig. 2.1. And gate using gdi technique

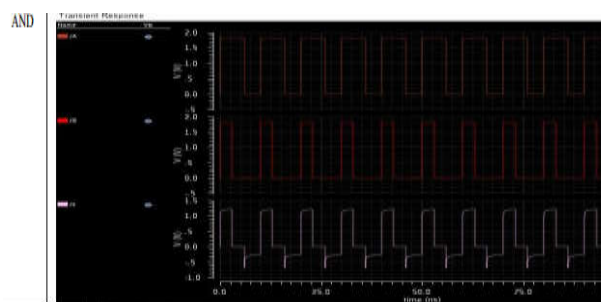


Fig 2.2. Transient response of AND gate using GDI technique.

DESIGN OF ALU USING GDI TECHNIQUE

In digital system design processor is main part of the system. And an ALU is one of the main components of a microprocessor. CPU works as a brain to any system & and ALU works as a brain to CPU. So it's a brain of computer's brain. They consists of fast dynamic logic circuits and description of ALU. Fig 2 shows the RTL design of ALU components using conventional CMOS. Fig 3 shows the chip design of ALU, Fig 4 shows inside the chip design. From Fig V it shows the Timing and Power analysis for the ALU using GDI and Fig 3.10 it shows the final Logic diagram for the ALU using GDI technique in 45 nm technology.

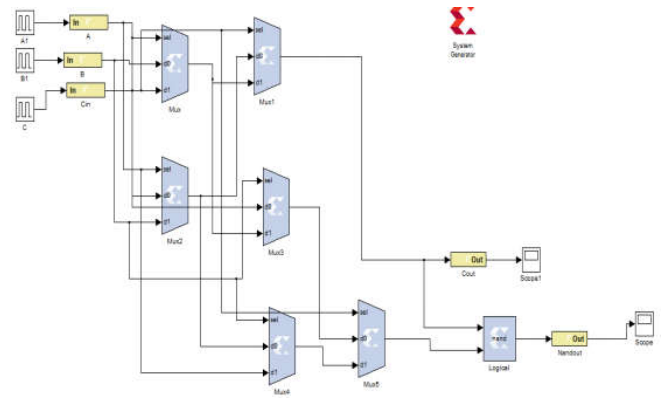


Fig 3.1. The design of ALU by using GDI technique

RTL SCHEMATIC

In digital circuit design, register-transfer level (RTL) is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers, and the logical operations performed on those signals. Here this RTL schematic shows the ALU using GDI.

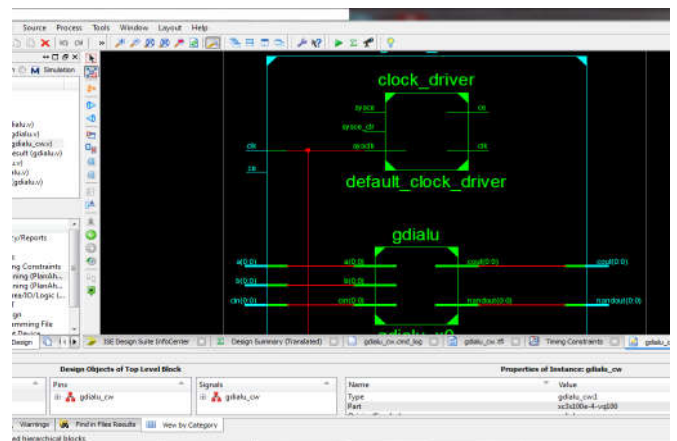


Fig 3.1.1: RTL Schematic of ALU

CHIP DESIGN

An ASIC (application-specific integrated circuit) is a microchip designed for a special application, such as a particular kind of transmission protocol or a hand-held computer. You might contrast it with general integrated circuits, such as the microprocessor and the random access memory chips in your PC..Here it shows the ALU chip design.

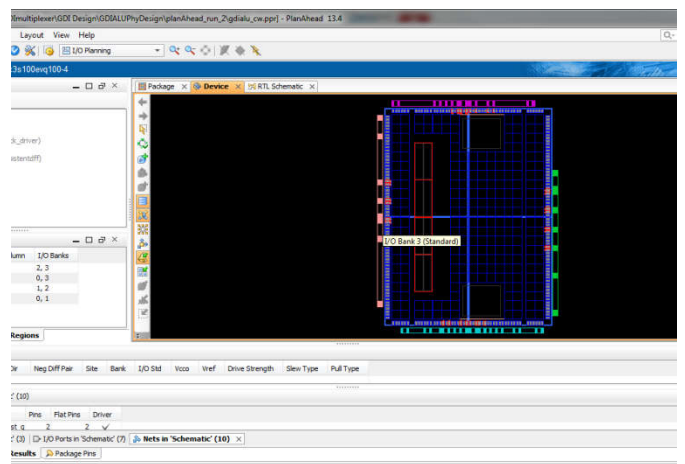


Fig 3.1.2: Chip Design of ALU

INSIDE THE CHIP

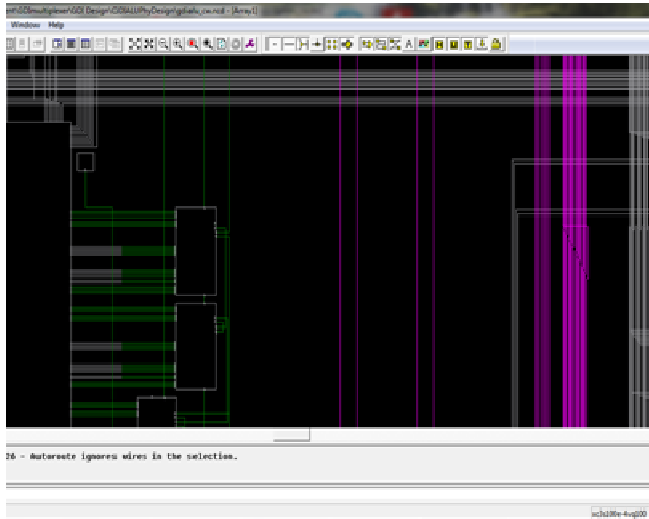


Fig 3.1.3: It shows the design inside the chip

TIMING ANALYSIS

Static timing analysis is a method of validating the timing performance of a design by checking all possible paths for timing violations without having to simulate. Timing is important because just designing the chip is not enough; we need to know how fast the chip is going to run, how fast the chip is going to interact with the other chips, how fast the input reaches the output etc...Timing Analysis is a method of verifying the timing performance of a design by checking for all possible timing violations in all possible paths.

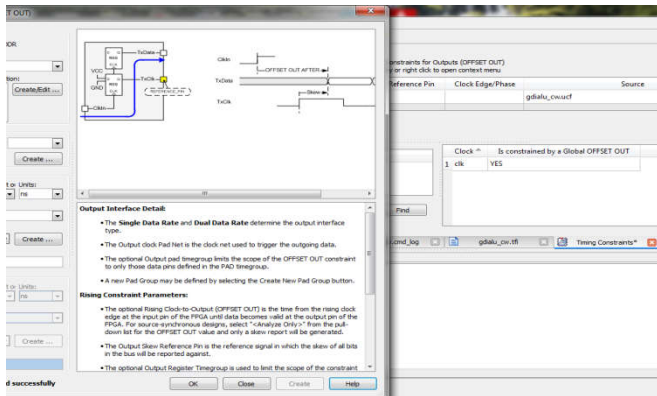


Fig 3.1.4: Timing Analysis

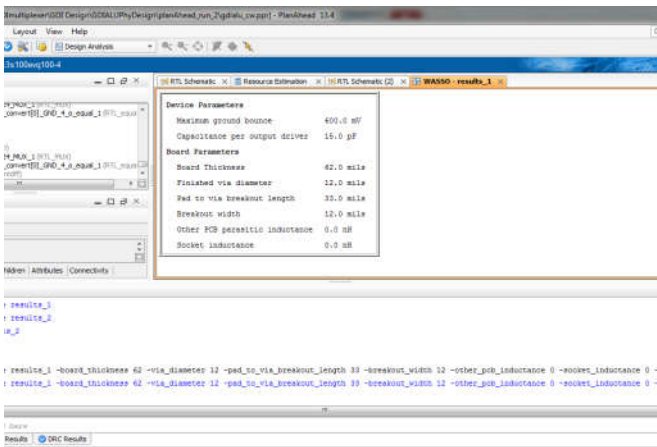


Fig 3.1.5: Noise Analysis

NOISE ANALYSIS

Noise Analysis is a small signal analysis which is carried out at discrete frequencies using a linearized version of the circuit. The mechanics are very similar to those of an AC analysis

P BLOCK ANALYSIS

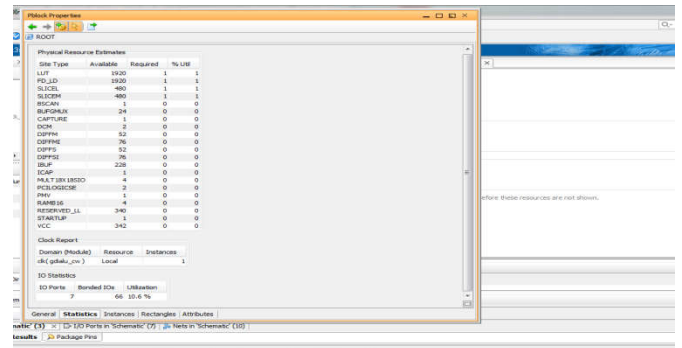


Fig 3.1.6. Physical Resource Estimation

TOTAL POWER ANALYSIS:

Power analysis is an important aspect of experimental design. It allows us to determine the sample size required to detect an effect of a given size with a given degree of confidence. Here the total power it used is 0.044W.

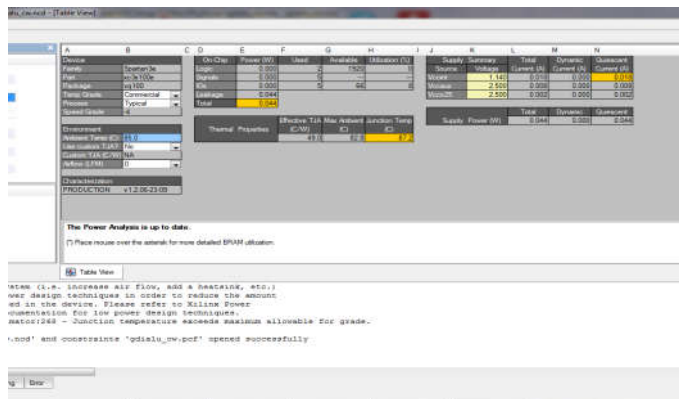


Fig 3.1.7. Power Analysis

RESOURCE UTILIZATION

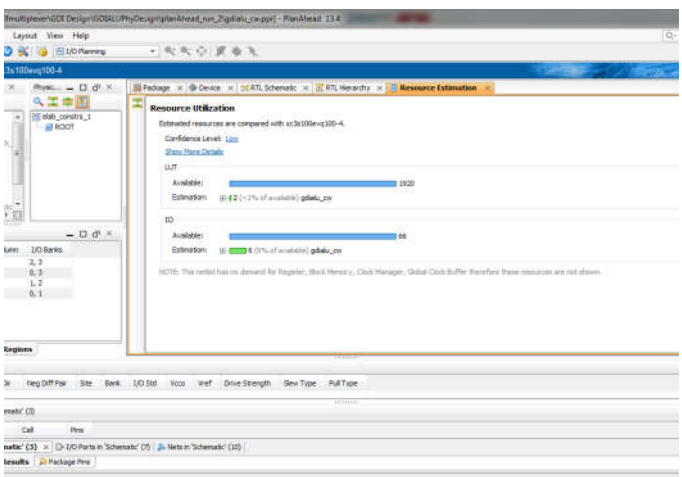


Fig 3.1.8. Resource Utilization

LOGIC DIAGRAM OF ALU USING GDI TECHNOLOGY

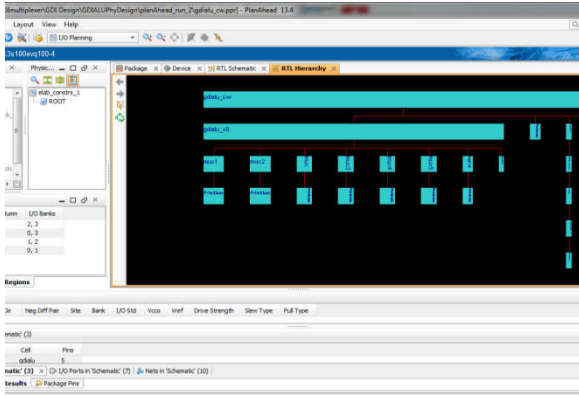


Fig 3.1.9: Logic Diagram of ALU

Comparison of simulation results of ALU using GDI and PTL

ALU Design	Using PTL	Using GDI
Power (uW)	0.000004471 W	0.044 W
Technology used (nm)	65 Nm	45 Nm

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